Amendments to the Claims

Please amend Claims 14, 16, 17, 21, 26, 27 and 29 as follows:

Listing of Claims

1. (Previously Presented) A method for adaptively updating coefficients in a filter for processing data, comprising the steps of:

   a) receiving a data sequence in the filter and processing the data sequence in accordance with the coefficients in the filter to produce a processed data sequence;

   b) separately filtering the data sequence with a first set of filter characteristics to generate a filtered data term for the coefficients;

   c) filtering the processed data sequence using a second set of filter characteristics, said second set of filter characteristics being structurally and/or functionally identical to said first set of filter characteristics;

   d) generating a filtered ideal processed data sequence from the processed data sequence using a third set of filter characteristics, said third set of filter characteristics comprising a subset of filter characteristics structurally and/or functionally identical to said first filter characteristics;

   e) generating a filtered error term for the coefficients from the filtered processed data sequence and the filtered ideal processed data sequence; and

   f) updating the coefficients in the filter of step a with each of said filtered data term and said filtered error term.

2. (Previously Presented) The method of Claim 1, wherein filtering the processed data sequence comprises convolving the processed data sequence with said second set of filter characteristics to generate the filtered processed data sequence.

3. (Previously Presented) The method of Claim 2, wherein generating the filtered error term comprises determining a difference between the filtered processed data sequence and the filtered ideal processed data sequence.

4. (Previously Presented) The method of Claim 3, further comprising (i) detecting a sequence of said processed data sequence, and (ii) convolving said sequence-detected processed data sequence with said third set of filter characteristics to generate said filtered ideal processed data sequence.

5. (Previously Presented) The method of Claim 1, wherein said first set of filter characteristics is identical to said second set of filter characteristics.

6. (Previously Presented) The method of Claim 1, wherein at least part of said third set of filter characteristics is identical to said first and second sets of filter characteristics.

7. (Canceled)

8. (Canceled)

9. (Previously Presented) The method of Claim 1, wherein generating the filtered ideal processed data sequence comprises further processing said processed data sequence with a sequence detector, and convolving said sequence-detected processed data sequence with the third set of filter characteristics.

10. (Original) The method of Claim 1, wherein each of said first and second sets of filter characteristics comprises an error filter.

11. (Original) The method of Claim 10, wherein said filtering further comprises transposing a channel response to generate at least a subset of said first set of filter characteristics.

12. (Original) The method of Claim 1, wherein said data sequence comprises a digital data signal.

13. (Previously Presented) The method of Claim 1, wherein said processing step a) comprises equalizing said data sequence, said processed data sequence comprises an equalized data signal, said filtered processed data sequence comprises a filtered equalized data signal, and said ideal filtered processed data sequence comprises an ideal filtered equalized data signal.

14. (Original) The method of Claim 1, wherein said first and second sets of filter characteristics are configured to minimize a dominant error type.

15. (Original) The method of Claim 14, wherein said dominant error type comprises a single bit error.

16. (Original) The method of Claim 15, wherein said first and second sets of filter characteristics are further configured to minimize a dibit error.

17. (Previously Presented) A computer-readable medium containing a set of instructions which, when executed by a signal processing device configured to execute computer-readable instructions, is configured to perform a method comprising:

processing a data sequence in accordance with coefficients in a filter to produce a processed data sequence;

separately filtering the data sequence with a first set of filter characteristics to generate a filtered data term;

filtering the processed data sequence using a second set of filter characteristics, said second set of filter characteristics being structurally and/or functionally identical to said first set of filter characteristics;

generating a filtered ideal processed data sequence from the processed data sequence using a third set of filter characteristics, said third set of filter characteristics comprising a subset of filter characteristics structurally and/or functionally identical to said first of filter characteristics;

generating a filtered error term for the coefficients from the filtered processed data sequence and the filtered ideal processed data sequence; and

updating the coefficients in the filter with each of said filtered data term and said filtered error term.

18. (Previously Presented) The computer-readable medium of Claim 17, wherein said coefficients are for an adaptive finite impulse response (FIR) algorithm.

19. (Currently Amended) The computer-readable medium of Claim 18, wherein said coefficients are derived from ~~comprises~~ a least-mean-squares (LMS) gradient algorithm.

20. (Previously Presented) The computer-readable medium of Claim 17, wherein said processing step a) comprises equalizing said data sequence.

21. (Previously Presented) The computer-readable medium of Claim 17, wherein generating the filtered ideal processed data sequence comprises (i) detecting a sequence of said processed data sequence, and (ii) convolving said sequence-detected, processed data sequence with said third set of filter characteristics.

22. (Previously Presented) The computer-readable medium of Claim 21, wherein generating said filtered error term comprises subtracting the ideal filtered processed data sequence from the filtered processed data sequence.

23. (Canceled)

24. (Canceled)

25. (Previously Presented) The computer-readable medium of Claim 17, wherein each of said first and second sets of filter characteristics comprises an error filter.

26. (Previously Presented) The computer-readable medium of Claim 17, wherein said method further comprises minimizing a dominant error type.

27. (Previously Presented) The computer-readable medium of Claim 26, wherein said dominant error type comprises a single bit error.

28. (Previously Presented) The computer-readable medium of claim 17, wherein said set of instructions comprises object code, source code and/or binary code.

29. (Previously Presented) The computer-readable medium of claim 17, wherein said set of instructions comprises digital code configured for processing by a digital data processor.

30-48. (Cancelled)

49. (Presently Amended) A signal processing architecture, comprising:

a) an equalizer configured to equalize and/or filter a data sequence in accordance with filter coefficients and provide an equalized data output;

b) ~~separately~~ a separate first filter, configured to receive said data sequence and generate a filtered data term for updating said filter coefficients; and

c) an error term circuit, configured to receive said equalized data output and provide a filtered error term for updating said filter coefficients of part a from a filtered equalized data output and a filtered ideal equalized data output, said error term circuit comprising a second filter having filter characteristics structurally and/or functionally identical to said first filter, configured to filter said equalized data

output; a signal processor configured to provide an ideal equalized data output from the equalized data output; and a third filter configured to filter said ideal equalized data output, having a subset of filter characteristics structurally and/or functionally identical to said first filter.

50. (Original) The architecture of claim 49, wherein said equalizer comprises an adaptive finite impulse response (FIR) filter.

51. (Previously Presented) The architecture of claim 50, wherein said filter coefficients are derived from a least-mean-square (LMS) algorithm.

52. (Canceled)

53. (Previously Presented) The architecture of claim 49, wherein said signal processor comprises a sequence detector.

54. (Previously Presented) The architecture of claim 49, wherein said error term circuit further comprises a target filter configured to receive an output from said signal processor and provide said ideal equalized data output.

55. (Canceled)

56. (Canceled)

57. (Canceled)

58. (Canceled)

59. (Canceled)

60. (Canceled)

61. (Previously Presented) The architecture of claim 49, wherein said second filter receives said equalized data output and provides said filtered equalized data output.

62. (Canceled)

63. (Previously Presented) The architecture of claim 49, wherein said third filter comprises a target filter.

64. (Previously Presented) The architecture of claim 63, wherein said third filter further comprises an error filter.

65. (Previously Presented) The architecture of claim 49, further comprising a subtractor or comparator configured to (i) receive said filtered equalized data output and said filtered ideal equalized data output, and (ii) provide said filtered error term.

66. (Original) The architecture of claim 65, wherein said subtractor or comparator comprises said subtractor, and said subtractor is further configured to subtract one of said filtered equalized data output and said ideal filtered equalized data output from the other of said filtered equalized data output and said ideal filtered equalized data output.

67. (Original) The architecture of claim 49, wherein each of said first and second filters comprises an error filter.

68. (Original) The architecture of claim 67, wherein each of said first and second filters further comprises a matched filter.

69. (Original) The architecture of claim 67, wherein said error filter is configured to minimize one or more dominant error types.

70. (Original) The architecture of claim 69, wherein said one or more dominant error types comprise a single bit error event.

71. (Original) The architecture of claim 49, further comprising a receiver configured to receive data from a magnetic storage medium and provide said data sequence.

72. (Previously Presented) The architecture of claim 49, wherein said second filter is identical to said first filter.

73. (Previously Presented) The architecture of claim 72, wherein a portion of said third filter is structurally and/or functionally identical to said first and second filters.

74-96. (Canceled)

97. (Original) A system for reading magnetically recorded data, comprising:
    a) the architecture of claim 49; and
    b) at least one receiver communicatively coupled to said architecture for receiving said first data sequence.

98. (Original) The system of claim 97, wherein said equalizer comprises an adaptive finite impulse response (FIR) filter.

99. (Previously Presented) The system of claim 98, wherein said filter coefficients are derived from a least-mean-square (LMS) algorithm.

100. (Previously Presented) The system of claim 97, wherein said signal processor comprises a sequence detector configured to receive said equalized data output and provide a sequence-detected equalized data output.

101. (Previously Presented) The system of claim 100, wherein said error term circuit further comprises a target filter configured to receive an output from said sequence detector and provide said ideal equalized data output.

102. (Previously Presented) The system of Claim 100, said third filter comprising a portion structurally and/or functionally identical to said first and second filters.

103. (Original) The system of Claim 102, wherein said third filter further comprises a target filter.

104. (Canceled)

105. (Canceled)

106. (Original) The system of claim 101, wherein said second filter receives said equalized data output and provides a filtered equalized data output.

107. (Previously Presented) The system of claim 106, wherein said error term circuit further comprises a fourth filter configured to receive said ideal equalized data output and provide a filtered ideal equalized data output.

108. (Previously Presented) The system of claim 107, further comprising a subtractor or comparator configured to (i) receive said filtered equalized data output and said filtered ideal equalized data output, and (ii) provide said filtered error term.

109. (Original) The system of claim 97, wherein each of said first and second filters comprises an error filter.

110. (Original) The system of claim 109, wherein each of said first and second filters further comprises a matched filter.

111. (Original) The system of claim 109, wherein said error filter is configured to minimize one or more dominant error types.

112. (Original) The system of claim 111, wherein said one or more dominant error types comprise a single bit error event.

113. (Previously Presented) The system of claim 97, wherein said second filter is identical to said first filter.

114. (Canceled)

115. (Original) A magnetic recording system, comprising:
   a) the system of Claim 97; and
   b) a magnetic storage device, communicatively coupled to said system.

116. (Original) The magnetic recording system of claim 115, wherein said magnetic storage device comprises a floppy disk, a CD-ROM, a magnetic tape or a hard disk drive.

117. (Previously Presented) The method of Claim 1, wherein said third set of filter characteristics comprises an error filter and a target filter.

118. (Previously Presented) The method of Claim 10, wherein said third set of filter characteristics comprises said error filter and a target filter.

119. (Previously Presented) The computer-readable medium of Claim 25, wherein said third set of filter characteristics comprises said error filter and a target filter.

120. (Previously Presented) The architecture of claim 67, wherein said third filter comprises an error filter.

121. (Previously Presented) The architecture of claim 120, wherein said third filter further comprises a target filter.

122. (Previously Presented) The architecture of claim 68, wherein said third filter comprises an error filter and a matched filter.

123. (Previously Presented) The architecture of claim 122, wherein said third filter further comprises a target filter.

124. (Canceled)

125. (Previously Presented) The architecture of claim 70, wherein said first and second filters are further configured to minimize a dibit error.

126. (Canceled)

127. (Canceled)

128. (Canceled)

129. (Canceled)

130. (Cancelled)

131. (Cancelled)

132. (Cancelled)

133. (Cancelled)

134. (Previously Presented) The computer-readable medium of Claim 17, wherein filtering the processed data sequence comprises convolving the processed data sequence with said second set of filter characteristics to generate the filtered processed data sequence.

135. (Cancelled)

136. (Cancelled)

137. (Cancelled)

138. (Cancelled)

139. (Cancelled)

140. (Cancelled)